

# Decimal Floating-Point Arithmetic IP Cores Family

An average computer user speeds up the applications by over twenty times and slashes the energy use to less than 5% if decimal hardware units are employed. Interest in decimal arithmetic increased considerably in recent years. This IP family presents new designs for decimal floating point (DFP) addition, multiplication, fused multiply-add, division, and square root. It stresses the importance of energy savings achieved by hardware implementations of the IEEE 754-2008 standard for decimal floating point.

SilMinds is the first company worldwide to discuss energy savings in DFP and the first to present a hardware implementation of a fused multiply-add. Our Newton-Raphson based divider is over three times faster than the similar design previously reported.

A small presentation for the decimal technology may be downloaded from [here](#)

## DFPA Family Cores

- DecAdd64 - Decimal Adder Unit supporting decimal64 format
- DecAdd128 - Decimal Adder Unit supporting decimal128 format
- DecMult64 - Decimal Multiplier Unit supporting decimal64 format
- DecMult128 - Decimal Multiplier Unit supporting decimal128 format
- DecFMA64 - Decimal Fused Multiplier Adder Unit supporting decimal64 format
- DecFMA128 - Decimal Fused Multiplier Adder Unit supporting decimal128 format
- DecDiv64 - Decimal Divider Unit supporting decimal64 format
- DecDiv128 - Decimal Divider Unit supporting decimal128 format
- DecSqrt64 - Decimal Square rooter Unit supporting decimal64 format
- DecSqrt128 - Decimal Square rooter Unit supporting decimal128 format

## Key Features

- Full IEEE-754-2008 compliance. Decimal64 (16 digits) and decimal128 (34 digits) formats support.
- Decimal Interchange format encoding with Densely Packed Decimal (DPD) coding support.
- Combinational or pipelined versions are available.
- 7 rounding modes support.
- Tested with over 200,000 test cases compliant with IEEE-754-2008 format.
- Full accuracy and precision support.
- Fully synthesizable with no internal tri-states.

## IP Deliverables

The IP deliverables are highly dependent on the type of licensing agreement and the business model. Depending on the negotiated business model, the following deliverables might be included.

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL/VERILOG test bench environment.
- Full test suites compliant with IEEE 754-2008 standard.
- Technical documentation
- HDL core specification.
- Datasheets.
- Synthesis scripts.
- Technical support.
- IP Core deployment support