



# Decimal Floating Point Arithmetic IP Cores Family

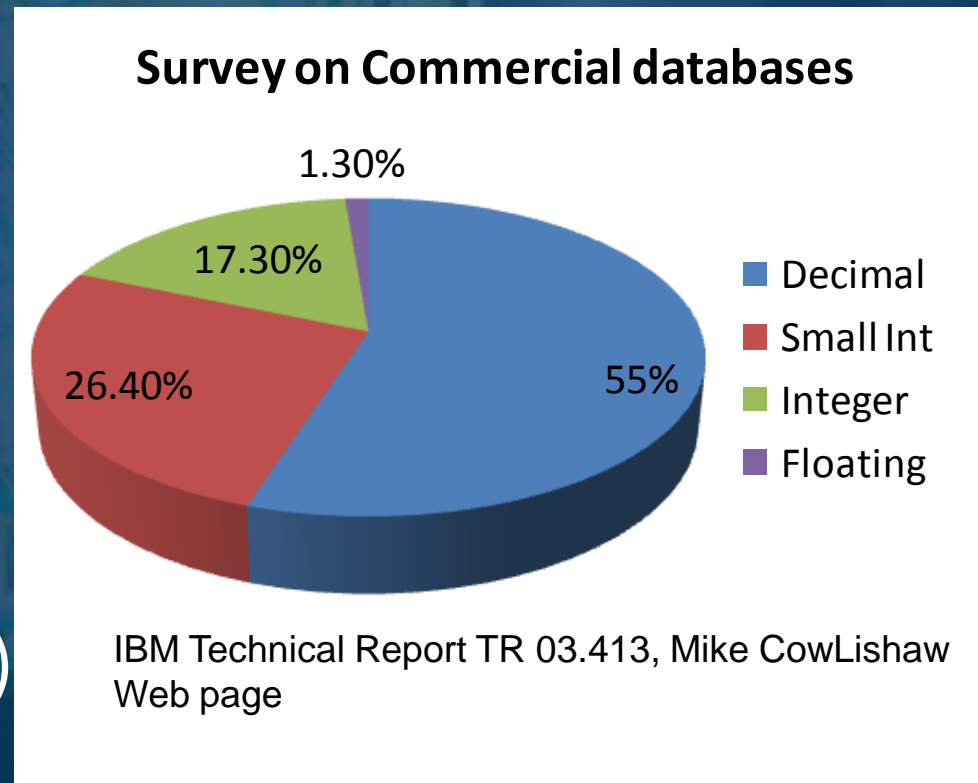
*Let the World Count Decimal*

# Agenda

- Why Decimal Arithmetic ?
- State of Affairs
- SilMinds DFPA IP Cores Family
- Performance Sample
- Features
- SilMinds

# Why Decimal Arithmetic ?

- Numbers are all decimal. (IBM Report)
- Currency conversion regulations dictate that 6 correct decimal digits must be present
- Loss of trailing zero if BFP is used ( $2.4 \neq 2.40$ )
- Loss of accuracy (endless fractions)



$$5\% = 0.05 = 0.000011001100110011 \dots$$

# Why Decimal Arithmetic ?

## Interest Calculation

- A saving bank certificate of value 80.9 USD and the annual interest rate is 5%
- Correct certificate value after one year is 84.945
- Correct rounded value is 84.94 (Banker's Rounding)
- Wrong Certificate value after one year (calculated on BFPU) = 84.9450000000000001
- Wrong rounded value = 84.95 (Banker's Rounding)
- Error is 1 cent per certificate.
- Bank will pay 1 more cent per certificate per year.
- Having millions of certificates may cause a big loss to the bank.

# State of Affairs

- Software decimal solutions
  - Fixed scale integers
    - Error prone
    - Fixed precision
    - Not IEEE 754r compliant
    - Higher precision requires huge disk space for storage.
    - Complex algorithms (slow)
    - Present in Oracle, Microsoft SQL, MySQL..etc.
  - Floating point packages
    - C decNumber and Intel SW library
    - Extremely slow (2 to 3 orders of magnitude slower than hardware)

# SilMinds DFPA IP Cores Family

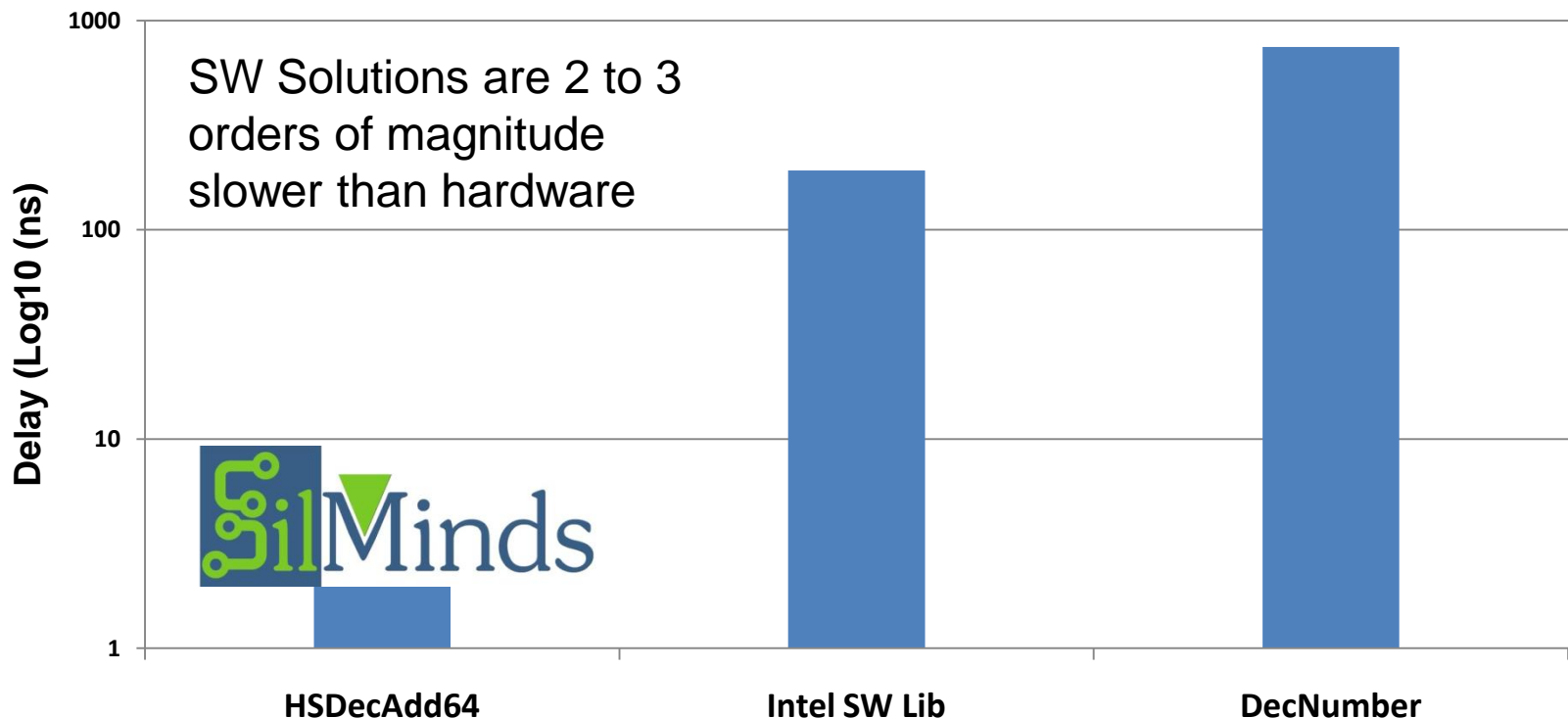
- Add/Subtract Cores
  - DecAdd64
    - HSDecAdd64 (High Performance)
    - LCDecAdd64 (Low Cost)
  - DecAdd128
    - HSDecAdd128 (High Performance)
    - LCDecAdd64 (Low Cost)
- Multiply Cores
  - DecMult64
    - HSDecMult64 (High Performance)
    - LCDecMult64 (Low Cost)
  - DecMult128
    - HSDecMult128 (High Performance)
    - LCDecMult128 (Low Cost)

# SilMinds DFPA IP Cores Family

- Fused Multiply Add Cores
  - DecFMA64
    - HSDecFMA64 (Q4-2008)
    - LCDecFMA64
  - DecFMA128
    - HSDecFMA128 (Q4-2008)
    - LCDecFMA128 (Q4-2008)
- Division Cores
  - DecDiv64
    - NRDecDiv64
    - DRDecDiv64 (Q4 – 2008)
  - DecDiv128 (Q4-2008)
- Square Root Cores
  - DecSqrt64
    - NRDecSqrt64
    - DRDecDiv64 (Q4-2008)
  - DecSqrt128 (Q4-2008)

# Performance Sample

## HSDecAdd64

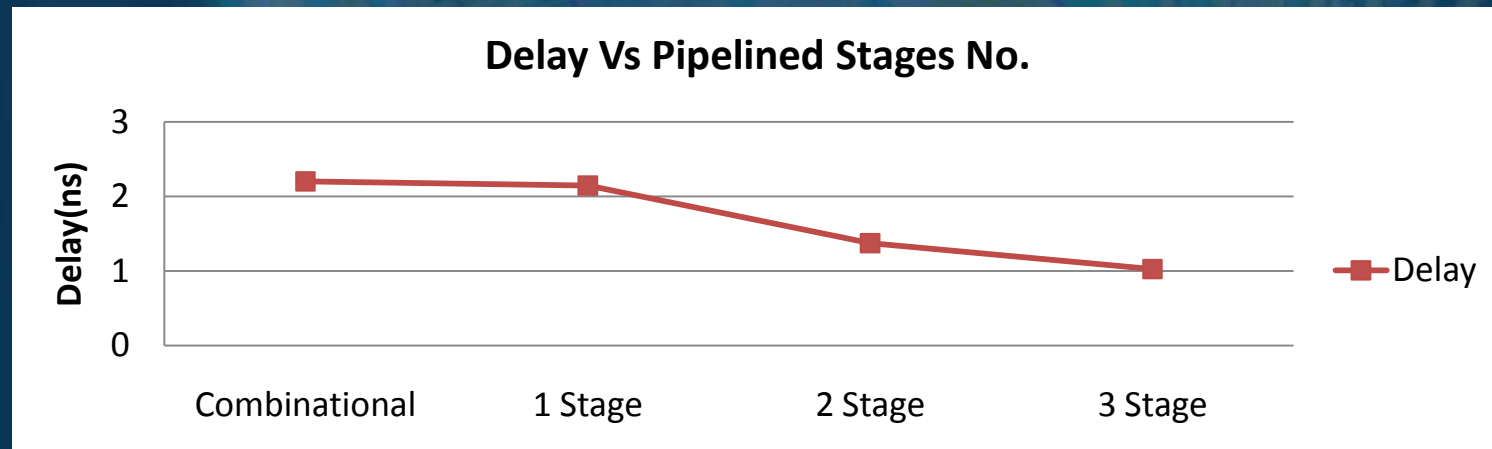


- 1- HSDecAdd64 was originally synthesized in 0.18 um technology and the delay was mapped into 90 nm technology.
- 2- The delay is post synthesis result.
- 3- Technology Mapping was done using 90ps , 45ps FO4 inverter delays for 0.18um , 90 nm technology respectively.
- 4- Software Testing was done on an Acer Aspire 5051 Laptop(AMD Turion , 2GHz, 2GB RAM, Ubuntu 8.04 OS)
- 5- The delay was originally computed in clock cycles and converted into time by multiplying it by 0.5 nS (2GHz Clock period, i.e. processor speed)

# Performance Sample

## HSDecAdd64

Format	Hardware Design	Area		Delay	
		$\mu\text{m}^2$	NAND2	ns	FO4
Dec-64	Combinational	200648.3	20106	4.4	48.9
	1 Stages	224801	22527	4.3	47.7
	2 Stages	236387.3	23687	2.75	30.5
	3 Stages	251346	25187	2.04	22.6



N.B.  
Original IP is synthesized in 0.18  $\mu\text{m}$  technology while the graph results are scaled to 90 nm technology

# Features

- Full IEEE-754r compliance.
- Decimal64 (16 digits) and decimal128 (34 digits) formats support.
- Decimal Interchange format encoding with Densely Packed Decimal (DPD) coding support.
- Combinational or pipelined versions are available.
- 7 rounding modes support.
- Tested with over 200,000 test cases compliant with IEEE-754r format.
- Full accuracy and precision support.
- Fully synthesizable with no internal tri-states.

# SilMinds

- Founded in 2007 as a silicon IP Design House
- Specialized in arithmetic hardware cores
- Provides Design services as well as IP cores
- High level of Know How (Stanford Ph.D., M.Sc's)